

Fig. 1A
(Prior Art)

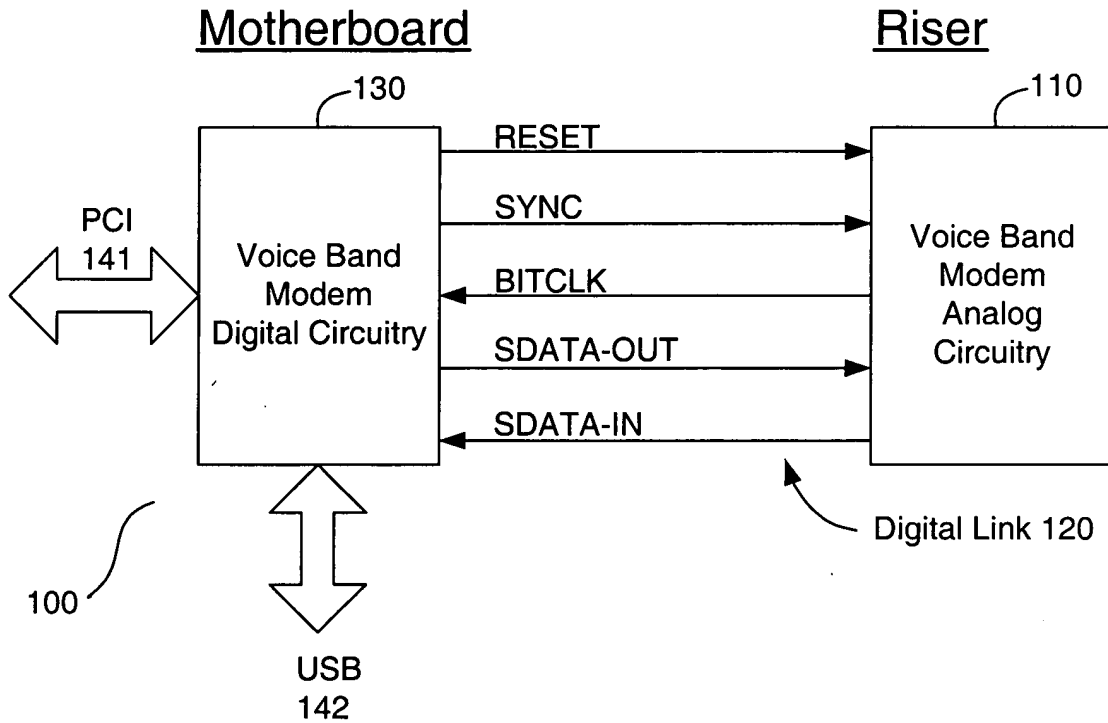


Fig. 1B

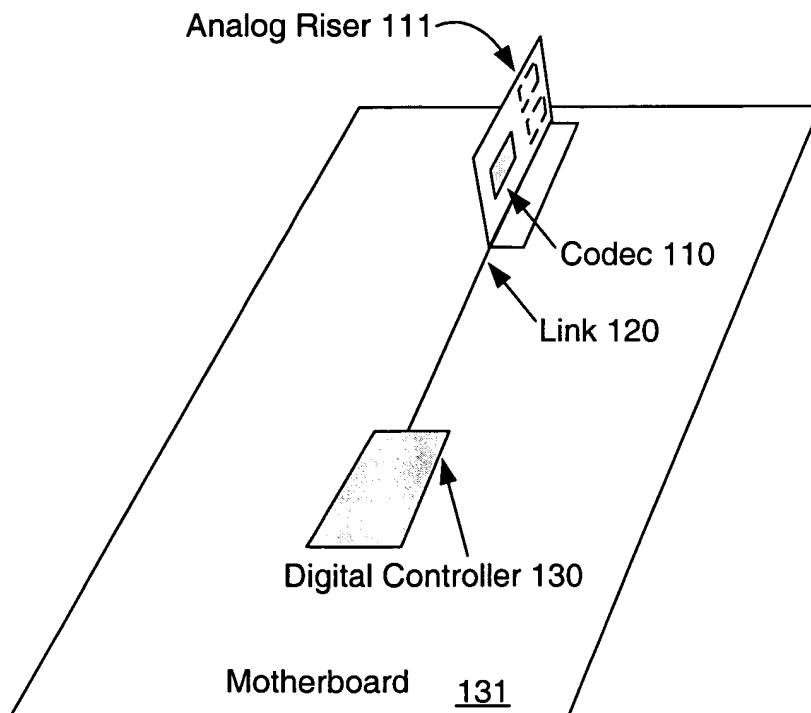


FIG. 1A is a block diagram of a prior art system.

Fig. 2A

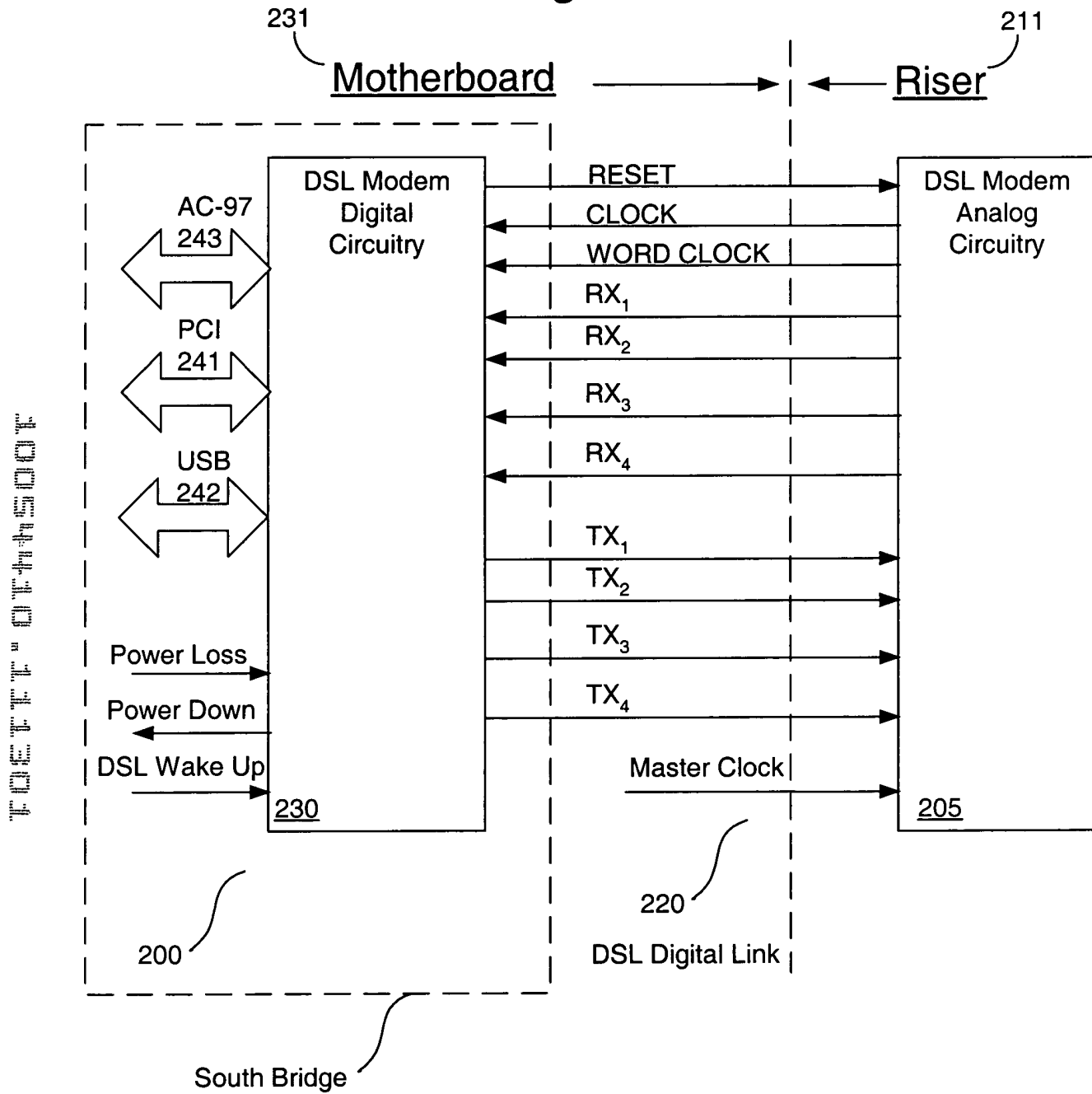


Fig. 2B-(Sheet 1)

Digital Section

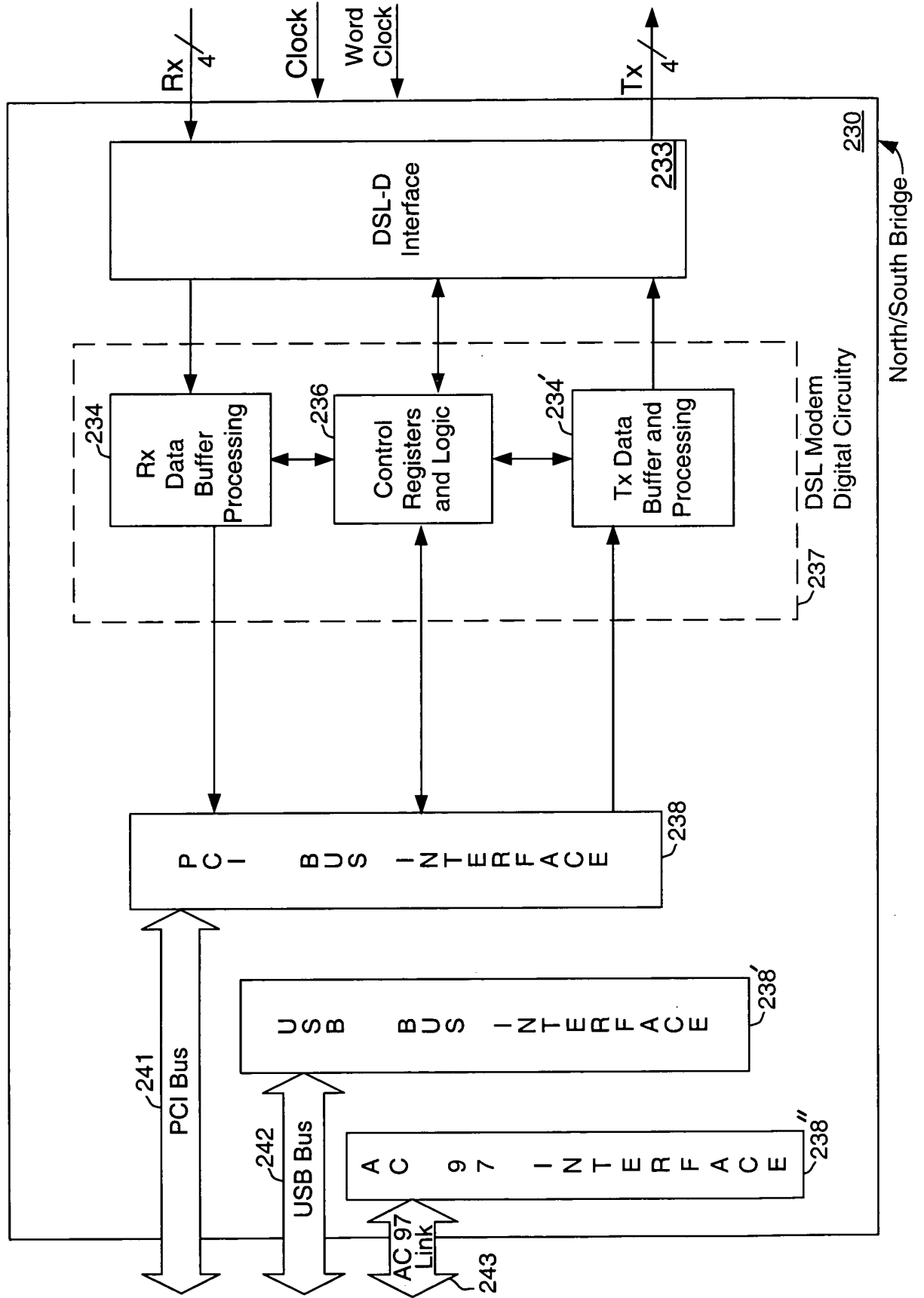


Fig. 2B-(Sheet 2)

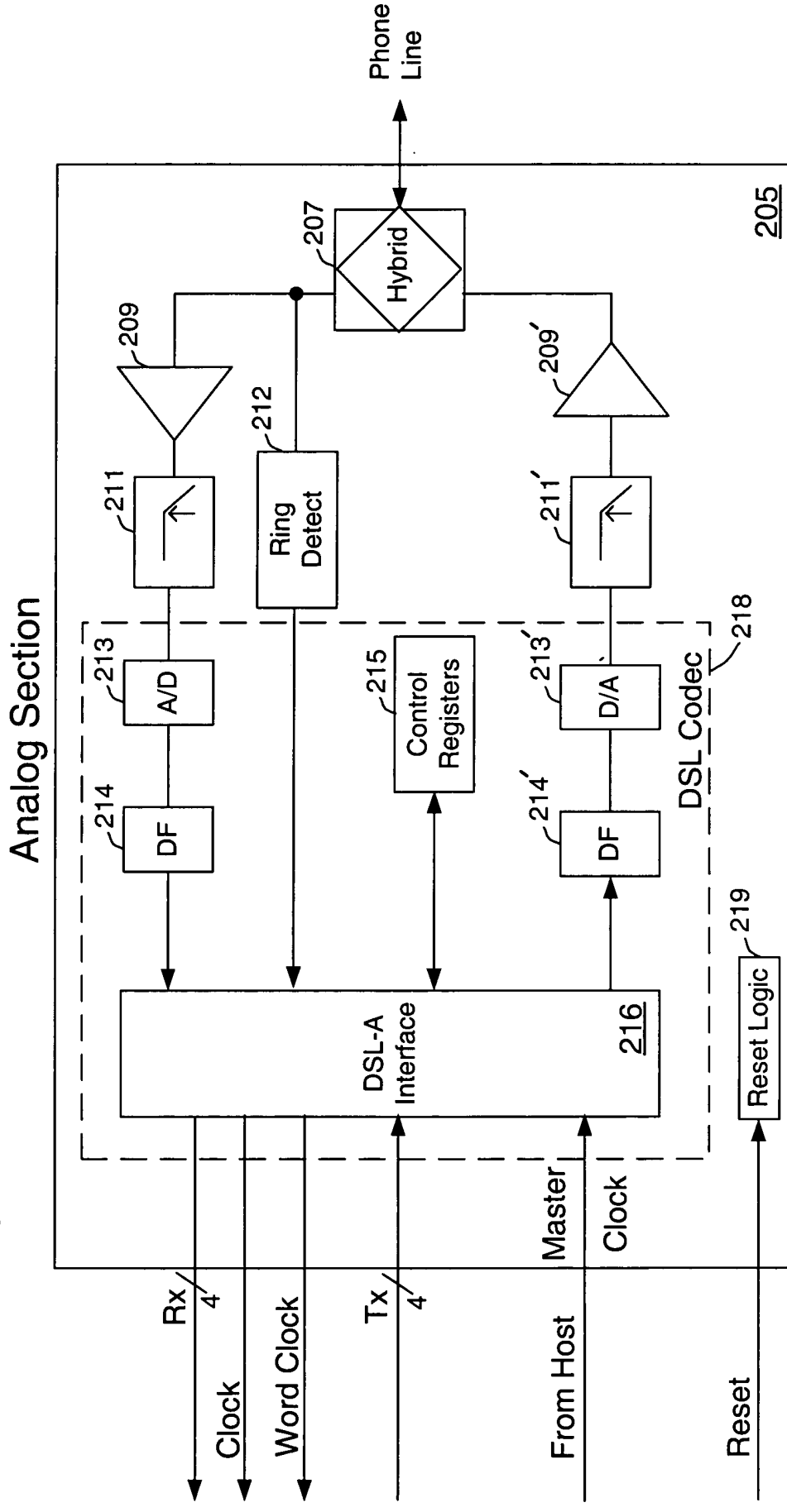


Fig. 3A

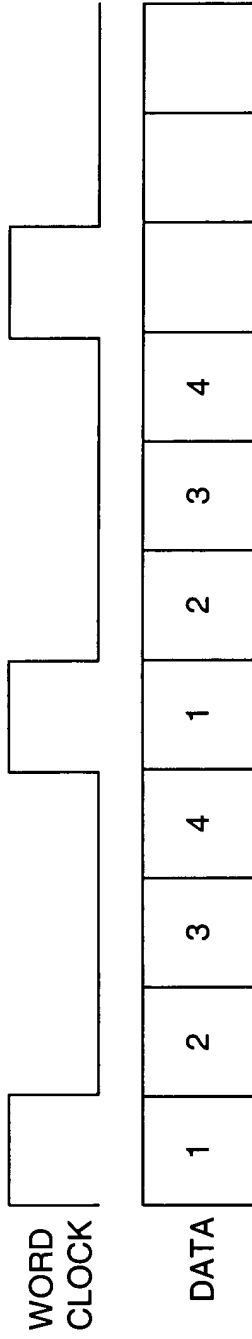


Fig. 3B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Cntl	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Fig. 3C

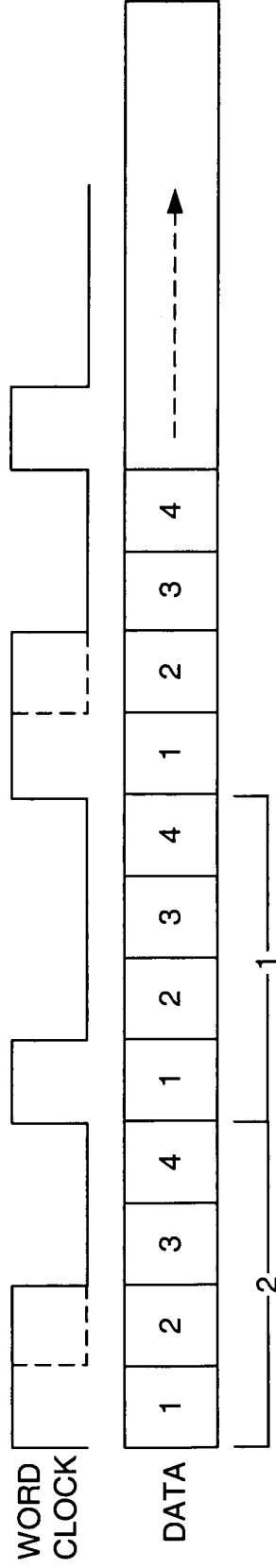


Fig. 4

DSL Link Pins	Cycle 1	Cycle 2	Cycle 3	Cycle 4
RxData[3:0]	Control, 0, RxClav, TxClav	RxSOC, RxAddr.[2:0]	RxData[7:4]	RxData[3:0]
TxData[3:0]	Control, 0, RxEnb, TxEnb	TxSOC, TxAddr.[2:0]	TxData[7:4]	TxData[3:0]